REMARKS

The following remarks are made in response to the Office Action mailed May 25, 2004. Claims 23-28, 30-45, 47 and 48 were rejected. Claims 29 and 46 have been objected to. With this Response, claims 25, 26, 29, 35, 42, and 46 have been amended. Claim 49 has been added. Claims 23-49 are pending in the application and are presented for reconsideration and allowance.

In the Specification

The title of the invention was objected to for not being descriptive. The title of the invention has been amended to "METHOD AND APPARATUS FOR BYTE ROTATION IN A DATA ALIGNMENT UNIT." Accordingly, the objection to the title has been traversed.

Claim Objections

Claim 35 is objected to because of informalities. Claim 35 has been amended to correct the informality. Accordingly, the objection to claim 35 has been traversed.

Claim 25 is objected to for insufficient antecedent basis. Claim 25 has been amended to include proper antecedent basis. Accordingly, the objection to claim 25 has been traversed.

Claims 26 and 42 are objected to for lacking support in the Specification. Claims 26 and 42 have been amended as suggested by the Examiner to overcome this objection. Accordingly, the objections to claims 26 and 42 have been traversed.

Claim Rejections under 35 U.S.C. § 103

Claims 23-25, 30-32, 34-36, 39-41, 43, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan U.S. Patent No. 5,638,369 ("Gaytan") in view of Bayliss U.S. Patent No. 4,407,016 ("Bayliss"). Applicant submits that Gaytan in view of Bayliss fails to disclose the invention of independent claims 23, 35, and 40.

Independent claim 23 recites a data alignment apparatus. The data alignment apparatus comprises an input for receiving an input temporal series of parallel-formatted input groups of digital data units, a data aligner coupled to said input and responsive to said input series for producing an output temporal series of parallel-formatted output groups of

said digital data groups, and an output coupled to said data aligner for outputting said output series. Said data aligner includes a buffer coupled to said input for storing data units of a first said input group while a second said input group is received at said input, and a combiner coupled to said buffer and said input for producing one of said output groups by combining in parallel format all of said data units stored in said buffer and selected data units of said second input groups. A data path is coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer.

Gaytan discloses a scalable packing circuit used to byte pack data transferred from a first storage element to a second storage element. The packing circuitry comprises a word packing circuit that receives data packets of a first bit width and stores them as data packets of a second bit width equivalent to the bit width of the second storage element. (See Abstract). Gaytan includes a bit packing circuit 650 comprising an input storage element 660, a bit rotate circuit 655, a save storage element 665, a selector 675, and an output storage element 670. (See fig. 6b). The input storage element 660 receives data from the word packing circuit 600 and routes data to both the save storage element 665 and the selector 675. The save storage element 665 delays data by a single cycle and outputs the data into selector 675. Thus, the selector 670 receives data input from both the input storage element 660 and the save storage element 665. (Col. 7, lines 21-31). Selector 675 includes four multiplexer groups 680, 685, 690, and 695 oriented in parallel to each other for collectively outputting one packed word of data at a time. (See figs. 6e-6f and col. 7, lines 44-48). The multiplexer groups 680, 685, 690, and 695 are selected by byte rotate circuit 655 via byte rotation select lines 656, which has the effect of selecting which inputs of each of the multiplexer groups 680, 685, 690, and 695 to pass for byte packing data from the word packing circuit. (Col. 8, lines 2-8).

Bayliss discloses a data processing system including a microprocessor providing an interface that allows a peripheral subsystem to access portions of main memory of a data processing system in a controlled and protected manor by means of address mapping facilities. (Col. 1, lines 8-14). A microprocessor receives addresses and data from a peripheral subsystem for use in subsequently accessing portions of the main memory of a data processing system in a controlled and protected manor. Each of the addresses is used to interrogate an associative memory to determine if the address falls within one of the sub-

ranges for a "window" on the main memory address space. If the address matches, then it is used to develop a corresponding address on the main memory address space. The data associated with the peripheral subsystem address is then passed through the interface and into the main memory at the translated memory address. Data transfer is improved by buffering blocks of data on the microprocessor. Data blocks are written into the buffer at a slower rate than data blocks are read out of the buffer and into main memory. A buffer bypass register allows single bytes of data to be transferred to a single address by bypassing the buffer. Address development and memory response signals are generated by the microprocessor rather than the peripheral subsystem processor for blocked transfers. (Abstract).

The Examiner conceded that Gaytan does not disclose a data path coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer. (See Office Action page 5). The Examiner submits that this limitation is taught by Bayliss in column 2, lines 25-31, which states: "Single bytes of data may be transferred to a single address by bypassing the buffer. This is accomplished by providing a buffer bypass register and allowing the microprocessor to operate in two modes, a random-access mode wherein the buffer is bypassed, and a block-transfer mode wherein the buffer is utilized."

Bayliss does not disclose **a data path coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer**. In contrast, Bayliss teaches a buffer 355 is 16 bits wide and is a transfer storage point between the GDP interface logic and the peripheral subsystem logic (See col. 23, lines 27-29). The buffer in Bayliss is not coupled to a combiner and an output for permitting an output group to be transferred to the output without being stored in the buffer. The buffer in Bayliss serves a different purpose and performs a different function than the buffer in the present invention. In view of the above, one skilled in the art could not combine the teachings of Gaytan and Bayliss and arrive at the present invention of independent claim 23.

Further, Gaytan and Bayliss fail to teach or suggest such a combination. Bayliss is directed to a microprocessor providing an interface between a peripheral subsystem and an object orientated data processor. Gaytan, in contrast, relates to a data packing circuit. Bayliss and Gaytan are in two separate technical areas. There is no teaching or suggestion in

Gaytan or Bayliss to combine the teachings of Bayliss with Gaytan to arrive at the present invention. In addition, Bayliss does not relate to a data alignment apparatus. In view of the above, Applicant respectfully submits that the above rejection of independent claim 23 under 35 U.S.C. 103(a) should be withdrawn.

Dependent claims 24-28 and 30-34 dependent directly or indirectly upon independent claim 23. Accordingly, dependent claims 24-28 and 30-34 are also allowable over the art of record.

Gaytan and Bayliss, either alone or in combination, also fail to disclose the claim recitations of independent claim 35. Claim 35 recites a data alignment method comprising receiving an input temporal series of parallel-formatted input groups of digital data units, in response to the input series, producing an output temporal series of parallel-formatted output groups of said digital data units, including storing data units of a first said input group in a buffer while a second said input group is received. Said producing step includes combining in parallel format all of said data units stored in the buffer and selected data units of said second input group to produce one of said output groups, and outputting said one output group for further processing without storing said one output group in the buffer.

Gaytan and Bayliss, either alone, or in combination, fail to disclose these claim recitations. As discussed above with reference to claim 23, Gaytan and Bayliss fail to disclose **outputting said one output group for further processing without storing said one output group in the buffer**. In view of the above, one skilled in the art could not combine the teachings of Gaytan and Bayliss and arrive at the present invention of independent claim 35. Accordingly, Applicant respectfully submits that the above rejection of independent claim 35 under 35 U.S.C. 103(a) should be withdrawn.

Dependent claims 36-39 depend directly or indirectly upon independent claim 35. Accordingly, dependent claims 36-39 are also allowable over the art of record.

Gaytan and Bayliss, either alone, or in combination, also fail to disclose the claim recitations in independent claim 40. Claim 40 recites an apparatus for interfacing a digital data processor to a digital communication network. The apparatus comprises a first data port that permits exchange of digital data with the data processor, a second data port that permits exchange of digital data with the communication network, and a data alignment apparatus coupled between said first and second data ports, including an input for receiving an input

temporal series of parallel-formatted input groups of digital data units, a data aligner coupled to said input and responsive to said input series for producing an output temporal series of parallel-formatted output groups of said digital data units, and an output coupled to said data aligner for outputting said output series. Said data aligner includes a buffer coupled to said input for storing data units of a first said input group while a second said input group is received at said input, and a combiner coupled to said buffer in said input for producing one of said output groups by combining in parallel format all of said data units stored in said buffer and select data units of said second input group. Said data alignment apparatus includes a data path coupled to said combiner and said output for permitting said one output group to be transferred to said output without being stored in said buffer.

For the same reasons as discussed above with reference to claim 23, Gaytan and Bayliss do not disclose these claim recitations. In view of the above, one skilled in the art could not combine the teachings of Gaytan and Bayliss and arrive at the present invention of independent claim 40. Accordingly, Applicant respectfully submits that the above rejection of independent claim 40 under 35 U.S.C. 103(a) should be withdrawn.

Dependent claims 41-45 and 47-48 depend directly or indirectly upon independent claim 40. Accordingly, dependent claims 41-45 and 47-48 are also allowable over the art of record.

Claims 26, 27, 37, 42 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan and Bayliss as applied to claims 23, 35 and 40 above, and further in view of Roskowski U.S. Patent No. 5,410,677 ("Roskowski"). Dependent claims 26 and 27 depend directly or indirectly upon independent claim 23. Accordingly, dependent claims 26 and 27 are also allowable over the art of record. Dependent claim 37 depends directly upon independent claim 35. Accordingly, dependent claim 37 is also allowable over the art of record. Dependent claims 42 and 44 depend directly or indirectly upon independent claim 40. Accordingly dependent claims 42 and 44 are also allowable over the art of record.

Claims 28, 33, 38 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaytan and Bayliss, as applied to claims 23 and 32 above, and further in view of well established teaching in the art. Dependent claims 28 and 33 depend directly or indirectly upon independent claim 23. Accordingly, dependent claims 28 and 33 are also allowable over the art of record. Dependent claim 38 depends indirectly upon independent claim 35.

Accordingly, dependent claim 38 is also allowable over the art of record. Dependent claim 45 depends indirectly upon independent claim 40. Accordingly, dependent claim 45 is also allowable over the art of record.

Allowable Subject Matter

The Examiner objected to claims 29 and 46 for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 29 and 46 have been rewritten in independent form including all the limitations of the base claim and any intervening claims. Therefore, Applicant believes claims 29 and 46 are allowable over the art of record.

Added Claims

Claim 49 has been added. Applicant believes added claim 49 to be allowable over the art of record.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 23-49 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 23-49 is respectfully requested.

Applicant hereby authorizes the Commissioner for Patents to charge Deposit Account No. 50-0471 in the amount of $190.00 to cover the fees as set forth under 37 C.F.R. 1.16(b)(c).

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 25 day of August, 2004.

By Steven E. Dicke
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